(12) PATENT APPLICATION PUBLICATION
(19) INDIA
(22) Date of filing of Application :26/03/2026

(21) Application No.202611036678 A
(43) Publication Date : 08/05/2026

(54) Title of the invention : AN EDGE COMPUTING ARCHITECTURE FOR LOW-LATENCY DATA PROCESSING

(51) International classification	:H04L 12/24, G06F 9/50, H04L 29/08, G06F 9/48, H04L 67/1095
(31) Priority Document No	:NA
(32) Priority Date	:NA
(33) Name of priority country	:NA
(86) International Application No Filing Date	: :01/01/1900
(87) International Publication No	: NA
(61) Patent of Addition to Application Number Filing Date	:NA :NA
(62) Divisional to Application Number Filing Date	:NA :NA

(71)**Name of Applicant :**
1)NOIDA INSTITUTE OF ENGINEERING & TECHNOLOGY
Address of Applicant :19, Knowledge Park-II, Institutional Area, Greater Noida – 201306, Uttar Pradesh, India. Uttar Pradesh India
(72)**Name of Inventor :**
1)TUSHAR
2)POOJA SHARMA

(57) Abstract :
An edge computing architecture for low-latency data processing comprises a source interface layer (101), an ingestion manager (102), a normalization engine (103), a priority classifier (104), a processing orchestrator (105), a low-latency analytics engine (106), a local response controller (107), a transient storage layer (108), an uplink policy manager (109), and a node coordination module (110). Data from local devices is ingested, normalized, prioritized, processed, and acted upon at an edge location, while selected information is temporarily retained and selectively synchronized with upstream systems to reduce response delay, bandwidth use, and dependence on remote cloud execution.

No. of Pages : 25 No. of Claims : 6